FERROELECTRIC MEMORY DEVICE AND METHOD OF READING A FERROELECTRIC MEMORY

ABSTRACT

A ferroelectric memory device comprises a plurality of subarrays having a plurality of bitlines and a plurality of wordlines crossing over the bitlines. Ferroelectric material is disposed between the wordlines and the bitlines to define a ferroelectric cell at each crossing of the wordlines and bitlines. Each subarray further comprises left and right voltage converters disposed on opposite sides thereof, to drive respective first and second sets of wordlines within the subarray. A plurality of global wordlines are couple to the left and right voltage converters of each subarray and are configured to establish the drive levels for respective wordlines of the subarrays. A bitline multiplexer selectively couples the bitlines of a select subarray to a plurality of sense amplifiers.